REMARKS

Claims 1-5, 7-12, 14, 15, 17, 19, 20, 22-27, 29, 31-33, 39, 40, 42, and 43 are pending. Claims 4 and 7-9 have been allowed, claims 2, 10-12, 23, 39, and 43 has been amended, and claims 6, 13, 16, 18, 21, 28, 30, 34-38, and 41 have been canceled. The amendment to claim 12 was made to incorporate the allowable subject matter of claim 16. It is therefore submitted that claim 16 is now allowable.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, claims 1, 3, 5, 17, 19, 22, 25, 34, 35 and 37-40 were rejected under 35 U.S.C. §102(b) being anticipated by the Uriu patent. This rejection is traversed for the following reasons.

Claim 1 recites a plurality of input/output ports for transmitting/receiving state information, and that "the state information is provided to each of the first and second boards through the input/output ports connecting the first board to the second board." (The port connections between the boards are illustratively shown in Fig. 3 of the drawings.) The Uriu patent does not disclose these features.

The Uriu patent discloses a control system for performing duplex operations between an active system and a standby system. The active system includes switchboard 21a and the standby system includes switchboard 21b. In operation, the standby board stores received ATM cells when the active board fails or otherwise becomes inoperative.

Unlike claim 1, the active sideboard 21a does not include input/output ports which communicate with input/output ports on standby board 21b. Instead, the Uriu patent makes clear that these boards operate independently from one another based on control information received from other circuits. That is, no port-to-port connections exist between the active and standby boards of Uriu, as recited in claim 1.

Also, because the Uriu boards do not have ports connecting one another, it logically follows that the Uriu boards do not send one another state information through input/output ports as is further recited in claim 1.

Also, claim 1 recites determining an active or standby state of the boards based on the state information communicated through the input/output ports between the boards. The Uriu patent does not disclose these features.

Because the Uriu patent does not disclose all the features recited in claim 1, it is respectfully submitted that the Uriu patent cannot anticipate claim 1 or any of its dependent claims.

Claim 19 recites that the state information communicated through the input/output ports connecting the boards determines "when the second board is required to assume the active state." The Uriu patent does not disclose the input/output ports of claim 1, and therefore fails to disclose the features of dependent claim 19.

Claim 22 recites "recognizing state information of a first and second duplexing control board by monitoring a plurality of input/output ports on each of the first and second duplexing control boards, wherein the state information is provided to each of the first and second boards through the input/output ports connecting the first and second duplexing control boards." Absent a disclosure of these features, it is respectfully submitted that the Uriu patent cannot anticipate claim 22 or any of its dependent claims.

Claim 25 recites features similar to those that patentable distinguish claims 1 and 22 from the Uriu patent, e.g., "recognizing state information of an opponent board from information of the input/output ports connecting the master board to the slave board, ... wherein the state information is provided to each of the master board and the slave board through the input/output ports connecting the master board and the slave board." The Uriu patent does not disclose these features and therefore cannot anticipate this claim or any of its dependent claims.

Claim 39 recites that "state information is transmitted through a pin-to-pin connection between the master and slave boards, and that the state information is used as a basis for switching a duplexing state of the slave board. The Uriu patent does not disclose these features.

Because the Uriu does not disclose all the features in the aforementioned claims, it is respectfully submitted that the §102(b) rejection should be withdrawn.

Claims 2, 10-14, 20, 23, 24, 26, 27, 29, 31-33, 41, and 42 were rejected under 35 U.S.C. §103(a) for being obvious in view of Uriu-Matsumura combination. This rejection is traversed for the following reasons.

Claim 2 recites "monitoring state information of first and second boards using the plurality of input/output ports, the input/output ports connecting the first and second boards by bypassing the input/output bus." As previously discussed, the Uriu patent does not teach or suggest that its active and standby boards have ports which are connected to one another. Without these ports, it is further evident that the Uriu patent does not monitor state information of the first and second boards using the plurality of input/output ports as recited in claim 1. To make up for these deficiencies, the Matsumura patent was cited.

The Matsumura patent discloses a duplexing system which includes an active side system and a standby side system. The active side system includes system switching control unit 21, and the standby side system includes system switching control 31. The Matsumura patent also discloses that the active and standby systems communicate with one another during a duplex operation. See column 4, lines 57-59.

Unlike claim 2, however, these active and standby systems do not have input/output ports connected to one another for exchanging state information. Instead, when a duplexing operation is to be performed, control units 21 and 31 exchange low-priority cells stored in buffers 20 and 30 respectively connected to the control units. See, for example, column 5, lines 35-46, which discloses in part: "The system-switching control units 21 and 31 mutually communicate each other and manage the temporary cell storage units 20 and 30, and **read out cells stored in both storage units...**". See also column 7, lines 1-15, which provides in part: "Inter-system communication section (213) communicates with inter-system communication

section of the other system **for arbitrating cell reading from which temporary cell storage unit is to be performed**...".

Thus, while the active and standby systems of the Matsumura patent communicate with one another during a duplexing operation, those systems only transfer low-priority cells stored in each of their buffers. The Matsumura patent does not teach or suggest that its active and standby systems include input/output ports which exchange state information from which an active or standby state of the boards can be determined. Absent a teaching or suggestion of these features, it is respectfully submitted that a Uriu-Matsumura combination cannot render claim 2 or any of its dependent claims obvious.

Applicants further submit that the claims subject to the §102(b) rejection are non-obvious for similar reasons, as each of these claims recite either directly or by virtue of their dependency input/output ports which connect the first and second boards of the duplex control system.

Claims 10 and 11 recite features similar to those which patentably distinguish claim 2 from the cited combination.

Claim 23 recites "a plurality of input/output ports to transmit state information of the duplexing control circuit and received state information from at least one other duplexing control circuit." This claim further recites that the state information is "provided to each of the duplexing control circuit and at least one other duplexing control circuit through the input/output ports...". These features are not taught or suggested by the Uriu and Matsumura patents, whether taken alone or in combination.

Claim 26 recites "a number of signal lines connecting ports on the master board and slave board, wherein the signal lines carry state information for switching duplexing between the boards." The Uriu and Matsumura do not teach or suggest these features. More specifically, the Uriu patent does not disclose any communication between its active and standby boards, and while the Matsumura patent discloses communication between its active and standby boards, only low-priority cells stored in respective buffers are exchanged between these boards. Matsumura does not teach or suggest transmitting state information between boards 21 and 31 through connected input/output ports.

Moreover, claim 26 recites that the state information "indicates a virtual path and a virtual channel for determining an active state and a standby state of the slave board and the master board." The Matsumura patent also fails to teach or suggest these features.

Based on at least these differences, it is respectfully submitted that claim and its dependent claims are allowable over a Uriu-Matsumura combination.

Claim 29 recites that the "state information includes a reset signal for resetting the master board when the master board switches to the standby state." Claim 29 therefore recites that the state information communicated through the number of signal lines recited in claim 26 includes a reset signal. The Matsumura patent does not teach or suggest these features. Accordingly, it is submitted that claim 29 is allowable not only by virtue of its dependency from claim 26 but also based on the features separately recited therein.

Claim 42 recites "transmitting a reset signal from the slave board to the master board when the state information indicates that master board has entered a standby state period." This claim depends from claim 39, which recites that the state information is "transmitted through a pin-to-pin connection between the master and slave boards." This pin-to-pin connection is not taught or suggested in the Uriu and Matsumura patents, whether taken alone or in combination. Therefore, the subject matter of claims 39 and 42 cannot be rendered obvious in view of the cited combination.

Claim 43 further defines the invention of claim 26 to include "a first port to inform the slave board of whether the master board is in the active state or standby state, a second port to inform the master board of whether the slave board is in the active state or standby state, a third port to output a reset signal from the master board to the slave board, and a fourth port to receive a reset signal for resetting the master board." None of the cited references teach or suggest these features.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this,

concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP

Daniel Y.J. Kim, Esq.
Registration No. 36,186

Samuel W. Ntiros, Esq.
Registration No. 39,318

P.O. Box 221200
Chantilly, Virginia 20153-1200
(703) 766-3701 DYK/SWN/lm
Date: December 16, 2005

Please direct all correspondence to Customer Number 34610